**INDEX**

|  |  |  |
| --- | --- | --- |
| Name: Mahesh Kumar Udas |  | Roll No.: 21 |
| Faculty: BSc.CSIT |  | Semester: Third |
| Subject: Computer Architecture |  | Year : Second |

|  |  |  |  |
| --- | --- | --- | --- |
| **S.N.** | **Title** | **Date of Submission** | **Sign** |
| **1.** | To design and simulate a 2-input AND gate using VHDL, and verify its functionality using a testbench. | **081/12/27** |  |
| **2.** | To design and simulate a 2-input OR gate using VHDL, and verify its functionality using a testbench. | **081/12/27** |  |
| **3.** | To design and simulate a NOT gate using VHDL, and verify its functionality using a testbench. | **081/12/27** |  |
| **4.** | To design and simulate a NAND gate using VHDL, and verify its functionality using a testbench. | **081/12/27** |  |
| **5.** | To design and simulate a **Half Adder Circuit** using VHDL, and verify its functionality using a testbench. | **081/12/27** |  |
| **6.** | To design and simulate a **Full** **Adder Circuit** using VHDL, and verify its functionality using a testbench. | **081/12/27** |  |