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| Subject: Computer Architecture |  | Year : Second |

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| **S.N.** | **Title** | **Date of Submission** | **Sign** |
| **1.** | To design and simulate a 2-input AND gate using VHDL, and verify its functionality using a testbench. | **2081/12/** |  |
| **2.** | To design and simulate a 2-input OR gate using VHDL, and verify its functionality using a testbench. | **2081/12/** |  |
| **3.** | To design and simulate a NOT gate using VHDL, and verify its functionality using a testbench. | **2081/12/** |  |
| **4.** | To design and simulate a NAND gate using VHDL, and verify its functionality using a testbench. | **2081/12/** |  |
| **5.** | To design and simulate a **Half Adder Circuit** using VHDL, and verify its functionality using a testbench. | **2081/12/** |  |
| **6.** | To design and simulate a **Full** **Adder Circuit** using VHDL, and verify its functionality using a testbench. | **2081/12/** |  |